

FACT™ Descriptions and Family Characteristics

Fairchild Semiconductor Advanced CMOS Technology —FACT—Logic

Fairchild Semiconductor introduced FACT™ (Fairchild Advanced CMOS Technology) logic, a family of high speed advanced CMOS circuits, in 1985.

FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability.

The 1.3-micron silicon gate CMOS process utilized in this family has been proven in the field of high performance gate arrays, CMOS ASIC, and FACT. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

In 1989, Fairchild Semiconductor introduced the FACT Quiet Series™ product line. This line of mostly octal bus-oriented logic functions is an enhancement of the original FACT line. Manufactured on a sub-micron silicon gate CMOS process, the FACT QS devices offer the lowest noise characteristics of any Advanced CMOS process with AC performance that is faster than FACT.

For direct replacement of LS, ALS and other TTL devices, the ACT and ACTQ circuits with TTL-type input thresholds are included in the FACT family.

Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACxx Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
 - Common Output Structure for Standard Gates and Buffer/Drivers
 - Output Sink/Source Current of 24 mA on AC/ACT and ACQ/ACTQ
 - Transmission Line Driving 50Ω Guaranteed
- Operation from 2V–6V V_{DD} Guaranteed (AC/ACQ)
- Temperature Range
 - 40°C to +85°C
- Improved ESD Protection Network
- High Current Latch-Up Immunity
- Patented Noise Suppression Circuitry on ACQ/ACTQ

Interfacing

FACT devices have a wide operating voltage range ($V_{DD} = 2 V_{DC}$ to $6 V_{DC}$, AC/ACQ) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

AC/ACQ— These are high speed CMOS devices with CMOS input switching levels and buffered CMOS outputs that can drive ± 24 mA of I_{OH} and I_{OL} current. Industry standard AC/ACQ nomenclature and pinouts are used.

ACT/ACTQ— These are high speed CMOS devices with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a $V_{DD} = 5V \pm 0.5V$ with $V_{OH} = 2.4V$ and $V_{OL} = 0.4V$, but are functional over the entire FACT operating voltage range of $2.0 V_{DC}$ to $5.5 V_{DC}$. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. ACT/ACTQ devices have the same output structures as AC/ACQ devices.

Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws 1000 times less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

FACT	= 0.1 mW/Gate
ALS	= 1.2 mW/Gate
LS	= 2.0 mW/Gate
HC	= 0.1 mW/Gate

FACT Product Comparison

Feature	FACT AC/ACT	FACT ACQ/ACTQ
Dynamic line driving guaranteed to switch on incident wave into transmission line impedance as low as 50Ω at +85°C	Yes $I_{OLD}/I_{OHD}: \pm 75 \text{ mA}$	Yes $I_{OLD}/I_{OHD}: \pm 75 \text{ mA}$
Guaranteed High Output Drive	$I_{OL}/I_{OH}: \pm 24 \text{ mA}$	$I_{OL}/I_{OH}: \pm 24 \text{ mA}$
Very High Speed Frequency	1 ns Internal Gate Delay; up to 100 MHz Toggle Frequency	≤1 ns Internal Gate Delay; up to 100 MHz Toggle Frequency
CMOS Power	5 μW/Gate	5 μW/Gate
CMOS Input Loading	±1 μA	±1 μA
Extended Operating Voltage Range	2.0V to 6.0V	2.0V to 6.0V
DC/AC Characteristics Guaranteed	3V and 5V ±10%	3V and 5V ±10%
Excellent Symmetrical Noise Margin (CMOS Inputs)	1.55V HIGH; 1.55V LOW	1.55V HIGH; 1.55V LOW
Dynamic Thresholds (TTL-Compatible Inputs)		Maximum 2.2V HIGH Minimum 0.8V (V_{IHD}); LOW (V_{ILD})
Guaranteed Latchup Immunity	±100 mA at +85°C	±300 mA at +85°C
ESD Immunity	Typical 6,000V	Typical 6,000V
Pin-to-Pin Output Propagation Delay Skew (Maximum)		1.0 ns (t_{OS}); Typical 0.5 ns
Guaranteed Output Noise Levels (Maximum)		1.5V V_{OLP} (Ground Bounce); -1.2V V_{OLV} (Undershoot)
Driving Force for JEDEC Standard for Advanced CMOS	Yes	
Inputs Compatible with: CMOS	AC	ACQ
TTL	ACT	ACTQ
Full Compatibility (Function, Part Number, Pinout) with Standard Functions	Yes	Yes (≥ 8 Bits)

Low Power CMOS Operation (continued)

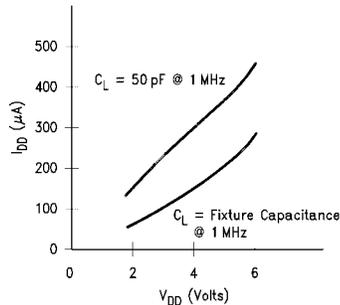


FIGURE 1. I_{DD} vs V_{DD}

Figure 1 illustrates the effects of I_{DD} versus power supply voltage (V_{DD}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays as well as the basic gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The examples below describe typical values for a 74XX138, 3-to-8 line decoder and a 74XX244 line driver.

138	
FACT AC	= 6.0 ns @ $C_L = 50$ pF
ALS	= 12.0 ns @ $C_L = 50$ pF
LS	= 22.0 ns @ $C_L = 15$ pF
HC	= 17.5 ns @ $C_L = 50$ pF

244	
FACT ACQ	= 4.0 ns @ $C_L = 50$ pF
FACT AC	= 5.0 ns @ $C_L = 50$ pF
ALS	= 7.0 ns @ $C_L = 50$ pF
LS	= 12.0 ns @ $C_L = 45$ pF
HC	= 14.0 ns @ $C_L = 50$ pF

AC performance specifications are guaranteed at 5.0V ± 0.5 V and 3.3V ± 0.3 V. For worst case design at 2.0V V_{DD} on all device types, the formula below can be used to determine AC performance.

AC performance at 2.0V $V_{DD} = 1.9 \times$ AC specification at 3.3V.

Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 5.0V $\pm 10\%$ V_{DD} .

Noise Immunity

The DC noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL} - V_{OL}|/|V_{IH} - V_{OH}|$ at 4.5V V_{DD} .

FACT	= 1.25V/1.25V
ALS	= 0.4V/0.7V
LS	= 0.3V/0.7V @ 4.75V V_{DD}
HC	= 0.8V/1.25V

Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both AC/ACQ and ACT/ACTQ device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All SSI and MSI devices (AC, ACT, ACQ or ACTQ) are guaranteed to source and sink 24 mA. 74AC/ACTxxx devices are capable of driving 50 Ω transmission lines.

I_{OL}/I_{OH} Characteristics

FACT AC/ACT	= 24 mA/-24 mA
FACT ACQ/ACTQ	= 24 mA/-24 mA
ALS	= 24 mA/-15 mA
LS	= 8 mA/-0.4 mA @ 4.75V V_{DD}
HC	= 4 mA/-4 mA

Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied "typical" output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these "typical" performance values across the operating voltage and temperature limits. Fortunately for the system designers, FACT has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50 Ω for the commercial temperature range.

Figure 2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ($I_{OUT} > 0$), are the V_{OH} and I_{IH} curves for FACT logic while on the left side ($I_{OUT} < 0$), are the curves for V_{OL} and I_{IL} . Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.

Dynamic Output Drive (continued)

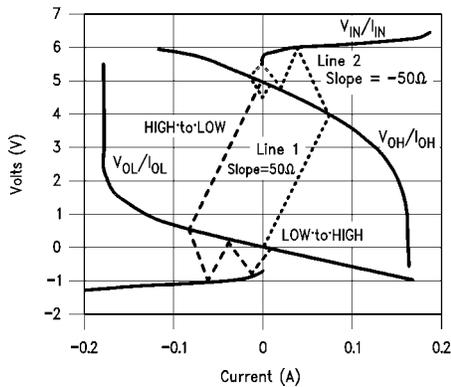


FIGURE 2. Gate Driving 50Ω Line Reflection Diagram

Begin analysis at the V_{OL} (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the V_{IN}/I_{IN} curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a 50Ω load line from this intersection to the V_{OH}/I_{OH} curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95V. Then draw a line with a slope of -50Ω from this first intersection point to the V_{IN}/I_{IN} curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the V_{IN}/I_{IN} curve will be waves travelling from the receiver to the driver.

Figure 3 through Figure 6 show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.

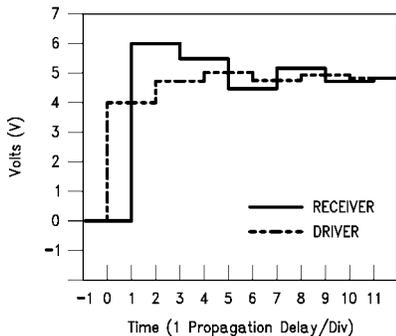


FIGURE 3. Resultant Waveforms Driving 50Ω Line—Theoretical

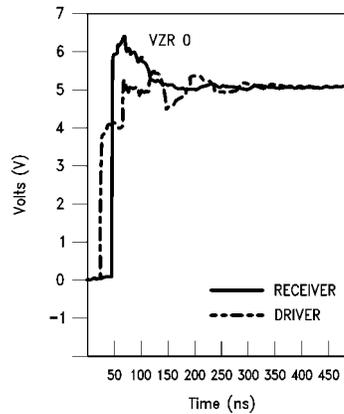


FIGURE 4. Resultant Waveforms Driving 50Ω Line—Actual

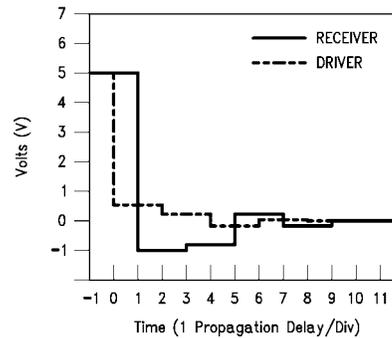


FIGURE 5. Resultant Waveforms Driving 50Ω Line—Theoretical

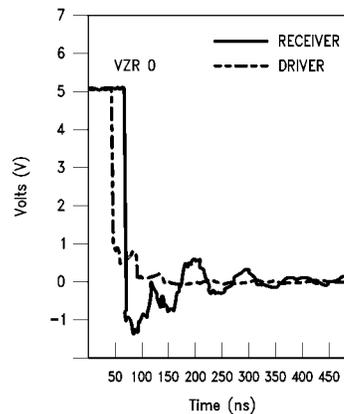


FIGURE 6. Resultant Waveforms Driving 50Ω Line—Actual

Dynamic Output Drive (continued)

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V_{DD} . The formula for calculating the current and voltage required is $|(V_{OQ} - V_I)/Z_O|$ at V_I . For $V_{OQ} = 100$ mV, $V_{IH} = 3.85$ V, $V_{DD} = 5.5$ V and $Z_O = 50\Omega$, the required I_{OH} at 3.85V is 75 mA. For the HIGH-to-LOW transition, $V_{OQ} = 5.4$ V, $V_{IL} = 1.65$ V and $Z_O = 50\Omega$, I_{OL} is 75 mA

at 1.65V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50Ω , the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA DC drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IN} level.

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

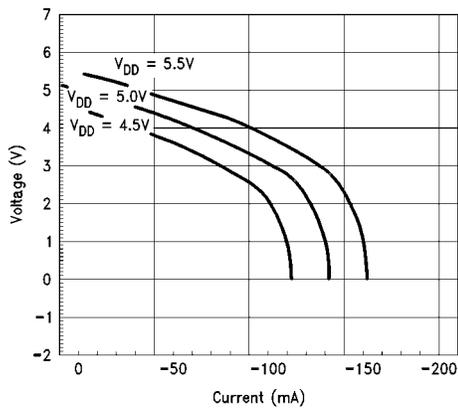


FIGURE 7. Output Characteristics V_{OH}/I_{OH} , AC00

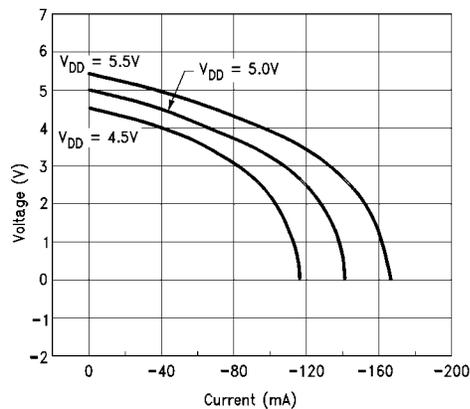


FIGURE 8. Output Characteristics V_{OH}/I_{OH} , ACTQ244

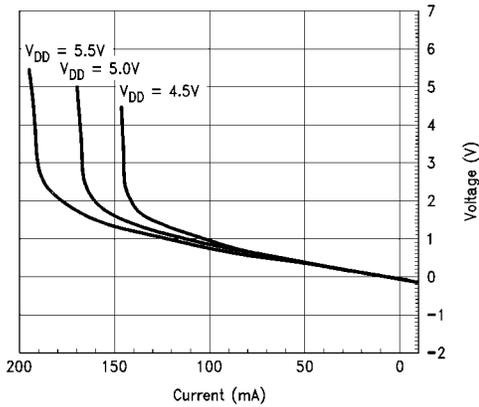


FIGURE 9. Output Characteristics V_{OL}/I_{OL} , AC00

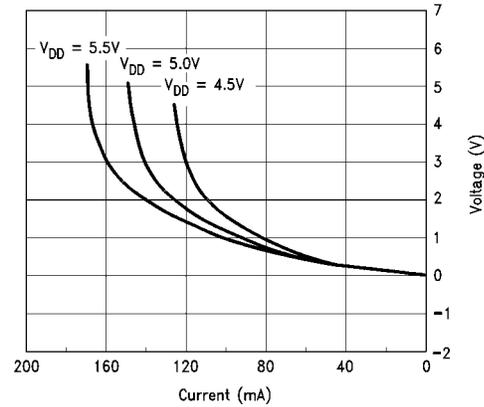


FIGURE 10. Output Characteristics V_{OL}/I_{OL} , ACTQ244

Dynamic Output Drive (continued)

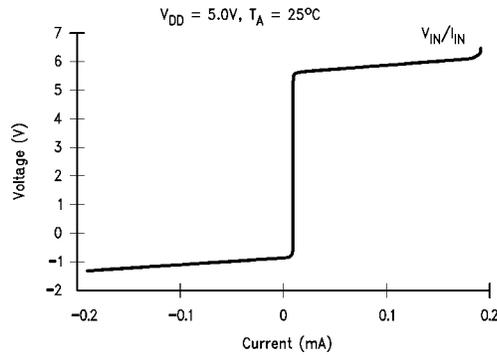


FIGURE 11. Input Characteristics V_{IN}/I_{IN}

Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish

interface standards for devices operating at $3.3V \pm 0.3V$. To this end, Fairchild Semiconductor guarantees all of its devices operational at $3.3V \pm 0.3V$. Note also that AC and DC specifications are guaranteed between 3.0V and 5.5V. Operation of FACT logic is also guaranteed from 2.0V to 6.0V AC/ACQ on V_{DD} .

Operating Voltage Ranges

FACT	= 2.0V to 6.0V (AC/ACQ)
FACT	= 5.0V \pm 10% (ACT/ACTQ)
ALS	= 5.0V \pm 10%
LS	= 5.0V \pm 5%
HC	= 2.0V to 6.0V

FACT Replaces Existing Logic

Fairchild Semiconductor's Advanced CMOS family is specifically designed to outperform existing CMOS and Bipolar logic families. Figure 12 shows the relative position of various logic families in speed/power performance. FACT

exhibits 1 ns internal propagation delays while consuming 1 μW of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

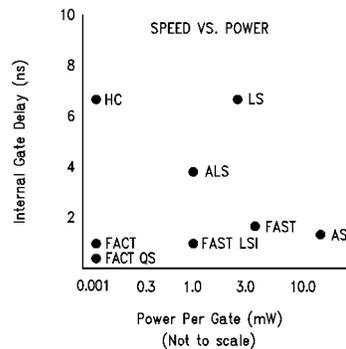


FIGURE 12. Internal Gate Delays

General Characteristics (All Max Ratings)

Symbol	Characteristics	ALS	HCMOS	FACT		Units
				AC/ACQ	ACT/ACTQ	
V _{CC/EE/DD}	Operating Voltage Range	5 ±10%	5 ±10%	5 ±5%	5 ±10%	V
T _A 74 Series	Operating	0 to +70	-40 to +85	-40 to +85	-40 to +85	°C
T _A 54 Series	Temperature Range	-55 to +125	-55 to +125	-55 to +125	-55 to +125	
V _{IH} (Min)	Input Voltage	2.0	3.15	3.85	2.0	V
V _{IL} (Max)	(Limits)	0.8	0.9	1.65	0.8	V
V _{OH} (Min)	Output Voltage	2.7	V _{DD} - 0.1	V _{DD} - 0.1	V _{DD} - 0.1	V
V _{OL} (Max)	(Limits)	0.5	0.1	0.1	0.1	V
I _{IH}	Input Current	20	+1.0	+1.0	+1.0	µA
I _{IL}		-200	-1.0	-1.0	-1.0	µA
I _{OH}	Output Current	-0.4	-4.0 @ V _{DD} - 0.8	-24 @ V _{DD} - 0.8	-24 @ V _{DD} - 0.8	mA
I _{OL}	at V _O (Limit)	8.0	4.0 @ 0.4V	24 @ 0.44V	24 @ 0.44V	mA
DCM	DC Noise Margin LOW/HIGH (V _{DD} = 4.5V)	0.4/0.7	0.8/1.25	1.25/1.25	0.7/2.4	V

Note 1: All DC parameters are specified over the commercial temperature range.

Speed/Power Characteristics (All Typical Ratings)

Symbol	Characteristics	ALS	HCMOS	FACT AC	Units
I _G	Quiescent Supply Current/Gate	0.2	0.0005	0.0005	mA
P _G	Power/Gate (Quiescent)	1.2	0.0025	0.0025	mW
t _{PD}	Propagation Delay (244 Typ.)	7.0	14.0	5.0	ns
	Speed Power Product	8.4	0.04	0.01	pJ
f _{MAX}	Clock Frequency D/FF	50	50	160	MHz

Propagation Delay

Symbol	Product		LS	ALS	HCMOS	FACT	Units
t _{PLH} /t _{PHL}	74XX00	Typ	10.0	5.0	8.0	5.0	ns
		Max	—	11.0	23.0	8.5	ns
t _{PLH} /t _{PHL} (Clock to Q)	74XX74	Typ	30.0	12.0	12.0	8.0	ns
		Max	—	18.0	44.0	10.5	ns
t _{PLH} /t _{PHL} (Clock to Q)	74XX163	Typ	27.0	10.0	20.0	5.0	ns
		Max	—	20.0	52.0	10.0	ns

Conditions: (LS) V_{DD} = 5.0V, C_L = 15 pF, 25°C;

(ALS/HC/FACT) V_{DD} = 5.0V ±10%, C_L = 50 pF, Over Temp, Max values at 0°C to +70°C for ALS, -40°C to +85°C for HC/FACT.

FIGURE 13. Logic Family Comparisons

Circuit Characteristics

POWER DISSIPATION

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Total power dissipation of FACT device under AC conditions is a function of three basic sources, quiescent power, internal dynamic power, and output dynamic power dissipation. Firstly, a FACT device will dissipate power in the quiescent or static condition. This can be calculated by using the formula: (Note: In many datasheets I_{DD} , ΔI_{DD} , I_{DDT} , and V_{DD} are referred to as I_{CC} , ΔI_{CC} , I_{CCT} , and V_{CC} , respectively. There are no differences.)

$$\text{Eq. 1 } PD_Q = I_{DD} \cdot V_{DD}$$

PD_Q = Quiescent Power Dissipation

I_{DD} = Quiescent Power Supply Current Drain

V_{DD} = Power Supply Voltage

Secondly, a FACT device will dissipate power dynamically by charging and discharging internal capacitance. This can be calculated by using one of the following two formulas:

$$\text{Eq. 2A (AC/ACQ)}$$

$$PD_{INT} = (C_{PD} \cdot V_S \cdot f) \cdot V_{DD}$$

PD_{INT} = Internal Dynamic Power Dissipation

C_{PD} = Device Power Dissipation Capacitance

V_S = Output Voltage Swing

f = Internal Frequency of Operation

V_{DD} = Power Supply Voltage

C_{PD} values are specified for each FACT device and are measured per JEDEC standards as described later on in Section 2. On FACT device data sheets, C_{PD} is a typical value and is given either for the package or for the individual stages with the device. (See Section 2). For FACT devices, V_S and V_{DD} are the same value and can be replaced by V_{DD}^2 in the above formula.

$$\text{Eq. 2B (ACT/ACTQ)}$$

$$PD_{INT} = [(I_{DDT} \cdot D_H \cdot N_T) \cdot V_{DD}] +$$

$$[(C_{PD} \cdot V_S \cdot f) \cdot V_{DD}]$$

PD_{INT} = Internal Dynamic Power Dissipation

I_{DDT} = Power Supply Current for a TTL HIGH

Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs HIGH

N_T = Number of TTL Inputs at D_H

V_{DD} = Power Supply Voltage

C_{PD} = Device Power Dissipation Capacitance

V_S = Output Voltage Swing

f = Internal Frequency of Operation

See Section 3 for more information on I_{DDT} or ΔI_{DD} .

Thirdly, a FACT device will dissipate power dynamically by charging and discharging any load capacitance. This can be calculated by using the following formula:

$$\text{Eq. 3 } PD_{OUT} = (C_L \cdot V_S \cdot f) \cdot V_{DD}$$

PD_{OUT} = Output Power Dissipation

C_L = Load Capacitance

V_S = Output Voltage Swing

f = Output Operating Frequency

V_{DD} = Power Supply Voltage

In many cases the output frequency is the same as the internal operation frequency. Also V_S is similar to V_{DD} and can be replaced by V_{DD}^2 . In the case of internal and output frequencies being identical Eq. 2A and Eq. 3 may be combined as follows:

$$\text{Eq. 4 } PD = (C_L + C_{PD}) \cdot V_{DD}^2 \cdot f$$

The total FACT device power dissipation is the sum of the quiescent power and all of the dynamic power dissipation. This is best described as:

$$\text{Eq. 5 } PD_{TOTAL} = PD_Q + PD_{DYNAMIC} \text{ OR}$$

$$PD_{TOTAL} = PD_Q + PD_{INT} + PD_{OUT}$$

The following is an exercise in calculating total dynamic I_{DD} for the FACT Advanced CMOS family. The device used as an example is the ACTQ374. Static I_{DD} , I_{DDT} and C_{PD} numbers can be found in the ACTQ374 data sheet. I_{DD} numbers used will be worst-case commercial guarantees. Room temperature power will be less. These are approximate worst-case calculations.

The following assumptions have been made:

- I_{DD} will be calculated per input/output (as per JEDEC C_{PD} calculations). The total for the ACTQ374 will be the calculated $I_{DD} \times 8$.
- Worst case conditions and JEDEC would require that the data is being toggled at the clock frequency in order to change the outputs at the maximum rate ($\frac{1}{2}$ CP).
- The data and clock input signals are derived from TTL level drivers (0V to 3.0V swing) at 50% duty cycle.
- The clock frequency is 16 MHz.
- I_{DD} will be calculated for $C_L = 50$ pF, 100 pF and 150 pF.
- $V_{DD} = 5V$.
- Total POWER dissipation can be obtained by multiplying total I_{DD} by V_{DD} (5.0V).
- Quiescent I_{DD} will be neglected in the total I_{DD} calculation because it is 1000 times less than dynamic I_{DD} .
- There is no DC load on the outputs, i.e. outputs are either unterminated or terminated with series or AC shunt termination.

Circuit Characteristics (continued)

The I_{DD} calculations are as follows:

$$I_{DD} \text{ Total} = \text{Input } I_{DD} + \text{Internal Switching } I_{DD} + \text{Output Switching (AC load) } I_{DD}$$

$$\begin{aligned} \text{Input } I_{DD} &= (I_{DDT}) \times (\text{number of TTL inputs}) \times (\text{Duty Cycle}) \\ &= (1.5 \times 10^{-3}) \times (1) \times (0.50) \\ &= 0.75 \text{ mA per input being toggled at TTL levels} \end{aligned}$$

$$\begin{aligned} \text{Internal } I_{DD} &= (V_{\text{SWING}}) \times (C_{\text{PD}}) \times (\text{CP freq}) \\ &= (5.0) \times (42 \times 10^{-12}) \times (16 \times 10^6) \\ &= 3.36 \text{ per mA per input being toggled by CP} \end{aligned}$$

$$\text{Output } I_{DD} = (V_{\text{SWING}} \times C_L) \times (\text{Q freq})$$

$$\begin{aligned} \text{a) } C_L &= 50 \text{ pF} \\ &= (5.0) \times (50 \times 10^{-12}) \times (8 \times 10^6) \\ &= 2 \text{ mA per output toggled at } \frac{1}{2} \text{ CP} \\ \text{b) } C_L &= 100 \text{ pF} \\ &= (5.0) \times (100 \times 10^{-12}) \times (8 \times 10^6) \\ &= 4 \text{ mA per output toggled at } \frac{1}{2} \text{ CP} \\ \text{c) } C_L &= 150 \text{ pF} \\ &= (5.0) \times (150 \times 10^{-12}) \times (8 \times 10^6) \\ &= 8 \text{ mA per output toggled at } \frac{1}{2} \text{ CP} \end{aligned}$$

Adding Input, Internal and Output I_{DD} together and multiplying by 8 I/O per ACTQ374, the approximate worst-case I_{DD} calculations are as follows:

$$C_L = 50 \text{ pF} \quad I_{DD} \text{ total} = 48.9 \text{ mA or } 244.5 \text{ mW}^* \text{ at CP} = 16 \text{ MHz}$$

$$C_L = 100 \text{ pF} \quad I_{DD} \text{ total} = 64.9 \text{ mA or } 324.5 \text{ mW}^* \text{ at CP} = 16 \text{ MHz}$$

$$C_L = 150 \text{ pF} \quad I_{DD} \text{ total} = 96.9 \text{ mA or } 484.5 \text{ mW}^* \text{ at CP} = 16 \text{ MHz}$$

Note: (*Power is obtained by multiplying I_{DD} by V_{DD})

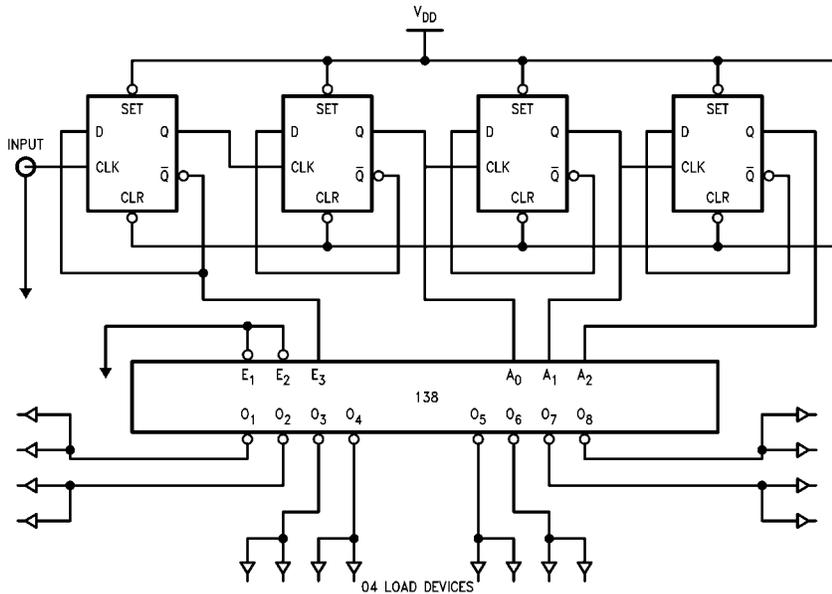


FIGURE 14. Power Demonstration Circuit Schematic

The circuit shown in Figure 14 was used to compare the power consumption of FACT versus FAST devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were

connected to the inputs of a '138 decoder. This generated eight non-overlapping clock pulses on the outputs of the '138, which were then connected to an '04 inverter. The input frequency was then varied and the power consumption was measured. Figure 15 illustrates the results of these measurements.

Circuit Characteristics (continued)

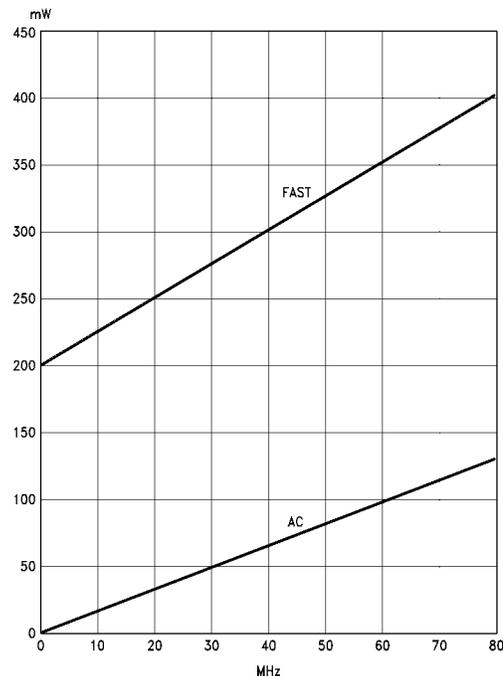


FIGURE 15. FACT vs FAST Circuit Power

The FACT circuit dissipates much less power than the FAST version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to zero; the FAST circuit continued to dissipate 200 mW.

SPECIFICATION DERIVATION

At first glance, the specifications for FACT logic might appear to be widely spread, possibly indicating wide design margins are required. However, several effects are reflected in each specification.

Figure 16 through Figure 18 illustrate how the data from the characterization of actual devices is transformed into the specifications that appear on the data sheet. This data is taken from the 'XX244.

Figure 16 shows the data taken (from one part) on a typical, single path, t_{PHL} , over temperature at 5.0V; there is negligible variation in the value of t_{PHL} . The next set of graphs, Figure 17 through Figure 18, depict data taken on the same device; these sets of curves represents the data on all paths. The data on this plot indicates only a small variation for t_{PHL} .

The graphs in Figure 16 through Figure 18 include data at 5.0V; Figure 19 shows the variation of delay times over the standard 5.0V $\pm 0.5V$ voltage range. Note there is only a $\pm 6\%$ variation in delay time due to voltage effects.

Now refer to Figure 20 which illustrates the process effects on delay time. This graph indicates that the process effects contribute to the spread in specifications more than any other factor in that the effects of the theoretical process spread can increase or decrease specification times by 30%. Because this 30% spread represents considerably more than ± 3 standard deviations, this guarantees an

increase in the manufacturability and the quality level of FACT product. To further ensure parts within specification will pass on testers at the limits of calibration, tester guardbands are incorporated.

With voltage and process effects added Figure 21 and Figure 22 the full range of the specification can be seen. For reference, the data sheet values are shown on the graph.

This linear behavior with temperature and voltage is typical of CMOS. Although the graphs are drawn for a specific device, other part types have very similar graphical representations. Therefore, for performance-critical applications, where not all variables need to be taken into account at once, the user can narrow the specifications. For example, all parts in a critically timed subcircuit are together on a board, so it may be assumed the devices are at the same supply and temperature.

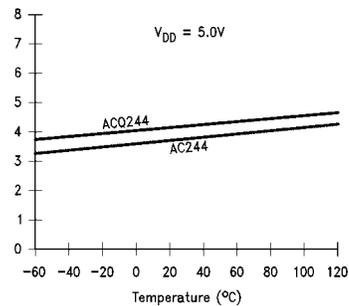


FIGURE 16. t_{PHL} Single Path

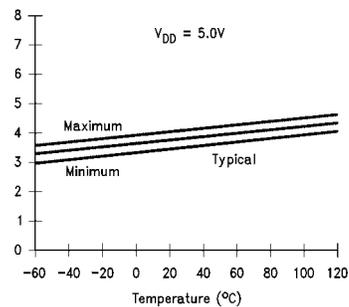


FIGURE 17. t_{PHL} , AC244, All Paths

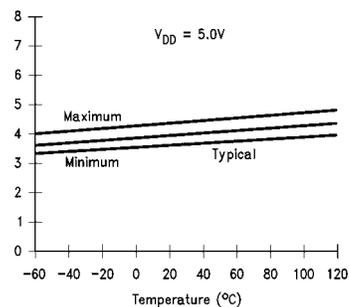


FIGURE 18. t_{PHL} , ACQ244, All Paths

Circuit Characteristics (continued)

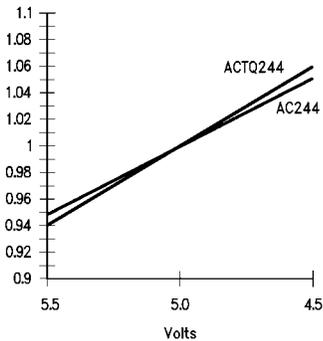


FIGURE 19. Voltage Effects on Delay Times

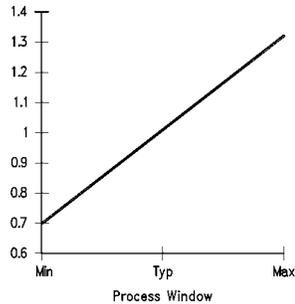


FIGURE 20. FACT Process Effects on Delay Times

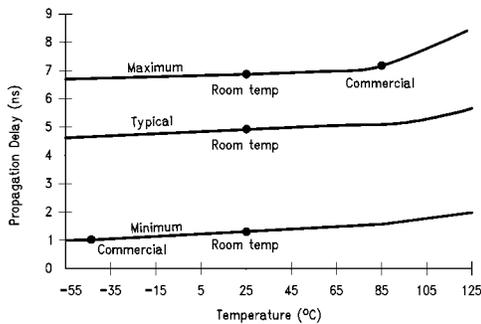


FIGURE 21. t_{PHL} , AC244, with Voltage and Process Variation

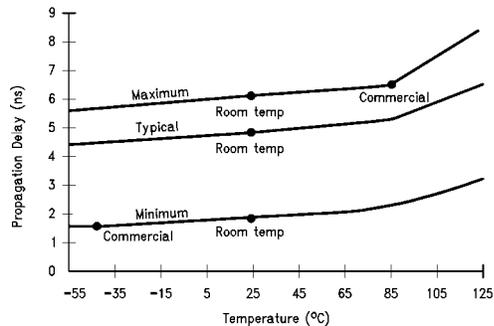


FIGURE 22. t_{PHL} , ACQ244, with Voltage and Process Variation

The same reasoning can be applied to setup and hold times. Consider the AC74. The setup time is 3.0 ns while the hold time is 0.5 ns. Theoretically, if these numbers were violated, the device would malfunction; however, in actuality, the device probably will not malfunction. Looking at the typical setup and hold times gives a better understanding of the device operation.

At 25°C and 5.0V, the setup time is 1.0 ns while the hold time is -1.5 ns. They are virtually the same; a positive setup time means the control signal to be valid before the clock edge, a positive hold time indicates the control signal will be held valid after the clock edge for the specified time, and a negative hold time means the control signal can transition before the clock edge. FACT devices were designed to be as immune to metastability as possible. This is reflected in the typical specifications. The true "critical" time where the input is actually sampled is extremely short: less than 50 ps.

By applying the same reasoning as we did to the propagation delays to the setup and hold times, it becomes obvious that the spread from setup to hold time (2.5 ns worst-case) really covers devices across the entire process/temperature/voltage spread. The real difference between the setup and hold times for any single device, at a specified temperature and voltage, is negligible.

CAPACITIVE LOADING EFFECTS

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Maximum delay numbers may be determined from the table below. Propagation delay are measured to the 50% point of the output waveform.

Parameter	Voltage (V)			Units
	3.0	4.5	5.5	
t_{PLH} FACT AC	31	22	19	ps/pF
FACT QS	34	19	19	
t_{PHL} FACT AC	18	13	13	ps/pF
FACT QS	32	22	20	

$T_A = 25^\circ\text{C}$

Figure 23, Figure 24 and Figure 25, Figure 26 describe propagation delays on FACT devices as affected by variations in power supply voltage (V_{DD}) and lumped load capacitance (C_L). Figure 27 and Figure 28 show the effects of lumped load capacitance on rise and fall times for FACT devices.

Circuit Characteristics (continued)

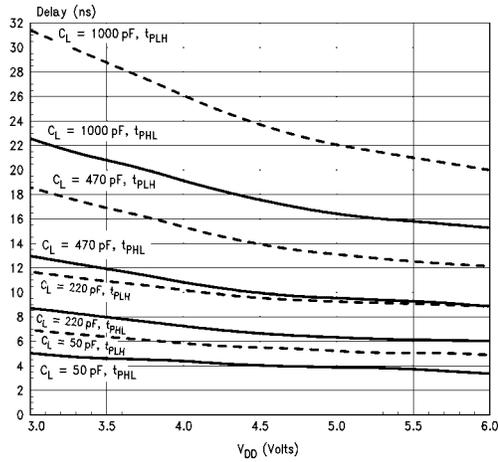


FIGURE 23. Propagation Delay vs V_{DD} (AC00)

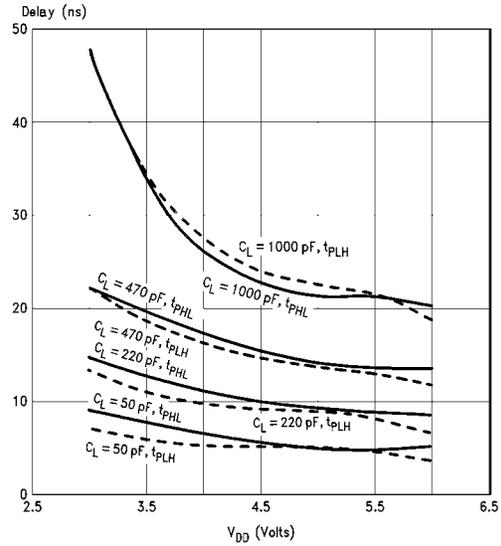


FIGURE 24. Propagation Delay vs V_{DD} (ACTQ244)

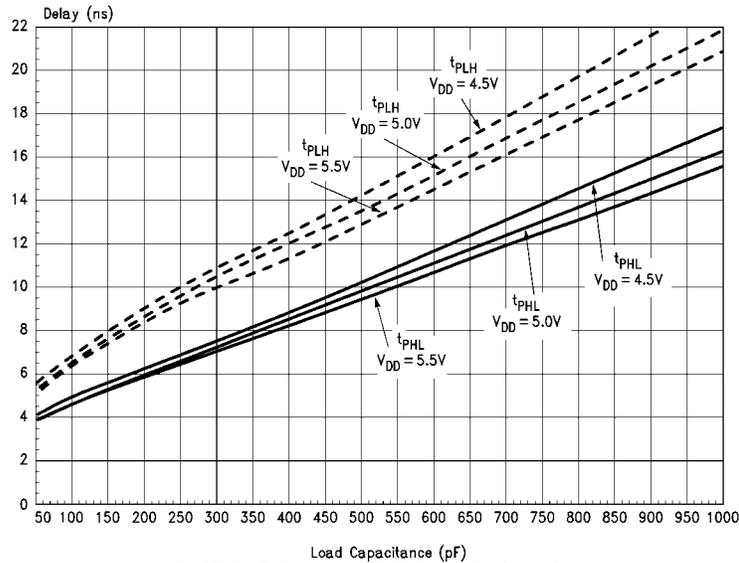


FIGURE 25. Propagation Delay vs C_L (AC00)

Circuit Characteristics (continued)

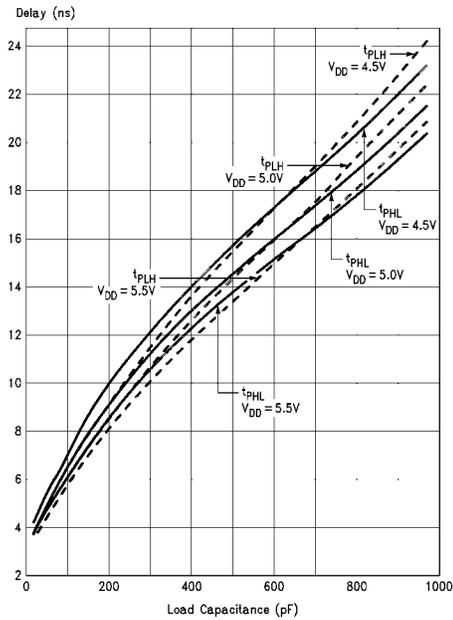


FIGURE 26. Propagation Delay vs C_L (ACTQ244)

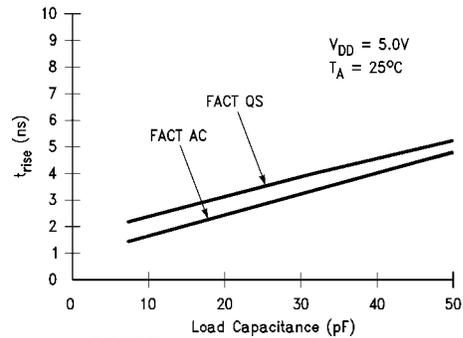


FIGURE 27. t_{rise} vs Capacitance

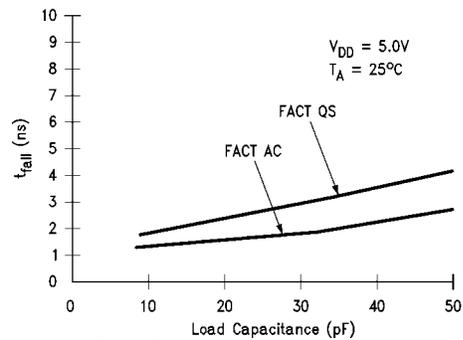


FIGURE 28. t_{fall} vs Capacitance

LATCH-UP

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA (300 mA for FACT QS) forced into or out of the inputs or the outputs under worst case conditions ($T_A = 125^\circ\text{C}$ and $V_{DD} = 5.5\text{ V}_{DC}$). At room temperature the parts can typically withstand dynamic currents of close to 1A. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

FACT devices have been specifically designed to reduce the possibility of latch-up occurring; Fairchild Semiconductor accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY

FACT circuits show excellent resistance to ESD-type damage. These logic devices are classified as category "B" of MIL-STD-883, test method 3015, and withstand in excess of 4000V typically. FACT logic is guaranteed to have 2000V ESD immunity on all inputs and outputs. Some FACT QS is guaranteed to have 4000V ESD immunity. FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 30 shows the ESD test circuit used in the sensitivity analysis for this specification. Figure 31 is the pulse waveform required to perform the sensitivity test.

Circuit Characteristics (continued)

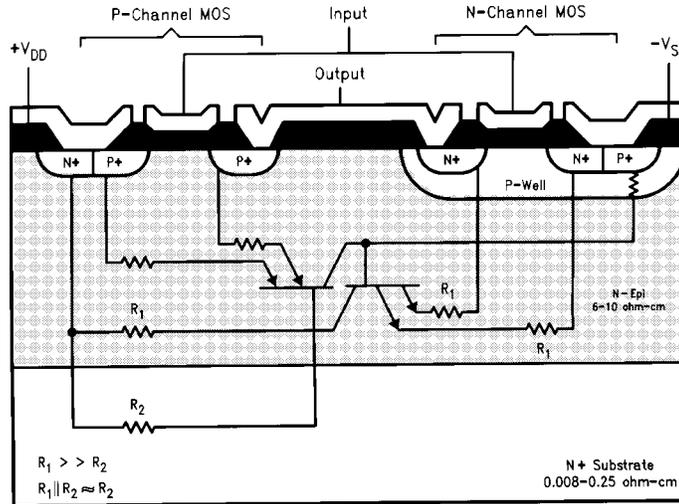


FIGURE 29. FACT EPI Process Cross Section with Latch-up Circuit Model

The test procedure is as follows; five pulses, each of at least 2000V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883. Devices that result in ESD immu-

nity in the 2000V-3999V range are listed as ESD Class 2. Devices that result in ESD immunity in the 4000+V range are listed as ESD Class 3. Several devices on the FACT QS are guaranteed as Class 3 (see individual data sheets). For further specifications, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.

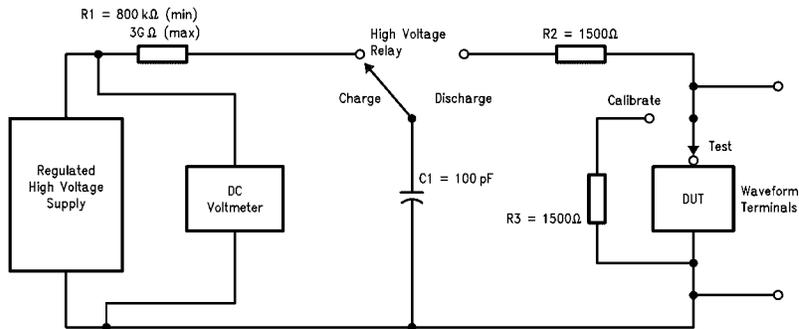


FIGURE 30. ESD Test Circuit

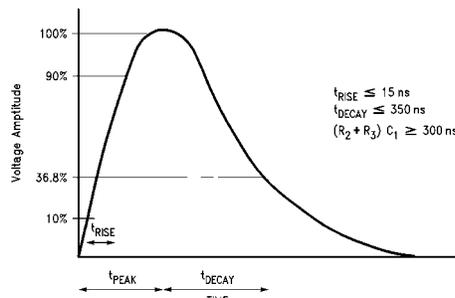


FIGURE 31. ESD Pulse Waveform

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